Please amend the paragraph beginning at page 8, line 11, deleting the underlining as follows:

~~BRIEF DESCRIPTION OF THE DRAWINGS~~

BRIEF DESCRIPTION OF THE DRAWINGS

Please amend the paragraph beginning at page 9, line 9, as follows:

DETAILED DESCRIPTION ~~OF A PREFERRED EMBODIMENT~~

Please amend the paragraph beginning at page 16, line 10, as follows:

~~This problem can be avoided by employing the additional circuitry~~ 630 illustrated in ~~Figure 9 in association with any~~ CID comparator 600 which may generate match signals directly, ~~i.e. without any further qualification by address. Accordingly, the output from the~~ CID comparator ~~600 is input to an~~ AND gate 620 which receives as its other input the output of NAND gate 610. This NAND gate 610 is ~~arranged to receive three signals, which indicate~~ whether the processor core is ~~operating in privileged mode, whether software debug is enabled,~~ and identify ~~when no further address comparison is being used to qualify the output of~~ CID comparator ~~600. As long as one of the three signals is not activated, NAND gate 610 will output~~ a logic one value, which will enable the match signal generated ~~by~~ the CID comparator 600 to be output directly as a match signal. ~~However, if all three~~ signals ~~are at a logic one level, i.e. the processor core is operating in privileged mode, software debug is enabled,~~ and no further address comparison is ~~being used,~~ then NAND gate 610 will output a logic zero value, which will prevent the output from CID comparator 600 from being issued ~~until such time as one of the~~ three inputs to the NAND gate is ~~de-asserted. The manner in which this~~ circuitry assists in avoiding the ~~problem illustrated in Figure 8A can be seen when considering Figure 8B.~~